



(19)

01217956 A

(11) Publication number:

Generated Document.

## PATENT ABSTRACTS OF JAPAN

(21) Application number: 63041948

(51) Intl. Cl.: H01L 27/04 H01L 21/205

(22) Application date: 26.02.88

(30) Priority:

(43) Date of application  
publication: 31.08.89(84) Designated contracting  
states:

(71) Applicant: FUJITSU LTD

(72) Inventor: MIENO FUMITAKE

(74) Representative:

**(54) CONDUCTOR LAYER,  
CAPACITOR USING  
CONDUCTOR LAYER AND  
MANUFACTURE THEREOF**

(57) Abstract:

**PURPOSE:** To obtain a conductor layer whose surface is flat, and a capacitor using said layer wherein electric field does not concentrate and dielectric strength is increased, by forming the conductor layer by using amorphous silicon containing no crystal grains.

CONSTITUTION: Mixed gas of disilane or trisilane or tetrasilane and oxygen is used as reaction gas. Vapor growth is performed by heating the above gas, and its temperature is as follows; 400-500°C in the case of disilane, 350-450°C in the case of trisilane, and 300-400°C in the case of tetrasilane. Thus a flat surface conductor layer composed of an amorphous silicon layer of excellent quality is formed on a substrate. By using the above manufacturing method, an amorphous silicon layer 6 is subjected to vapor growth on a MOS field effect transistor, and eliminated from the region except a region in contact with drain 4. After an insulating layer 7 is formed, it is eliminated from the region except a region on the amorphous layer 6.

After a conductor layer 8 like a polycrystalline silicon layer is formed, it is eliminated from the region except a region on the insulating layer 7, and a capacitor composed of the amorphous silicon layer 6, the insulating layer 7 and the conducting layer 8 is formed.

COPYRIGHT: (C)1989,JPO&Japio



